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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,494	08/03/2000	Salil R. Raje	MDS-P007	1465

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EXAMINER
LEVIN, NAUM B

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/632,494	Applicant(s) RAJE ET AL.	
	Examiner Naum B Levin	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36,70-81 and 94-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36,70-81 and 94-100* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *37-69 and 82-93* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Claims 37-47, 48-58, 59-69, 82-87, 88-93 (Group 2) withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, 13-24, 25-36, 70-75, 76-81, 94-95, 96-100 (Group 1), drawn to performing an IC design based on a timing analysis, classified in class 716, subclass 4.

II. Claims 37-47, 48-58, 59-69, 82-87, 88-93 (Group 2), drawn to the IC design optimization, classified in class 716, subclass 2.

Inventions 1-12, 13-24, 25-36, 70-75, 76-81, 94-95, 96-100 (Group 1) and 37-47, 48-58, 59-69, 82-87, 88-93 (Group 2) are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because Group 1 includes physical placement limitations. The subcombination has separate utility such as performing estimates of physical area placement.

Because these inventions are distinct for the reasons given above and have

acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Attorney Dennis S. Fernandez Reg. No. 34,160 on 08/28/02 a provisional election was made traverse to prosecute the invention of Group 1, claims 1-12, 13-24, 25-36, 70-75, 76-81, 94-95, 96-100. Affirmation of this election must be made by applicant in replying to this Office action. Claims 37-47, 48-58, 59-69, 82-87, 88-93 (Group 2) withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12, 13-24, 25-36, 70-75, 76-81, 94-95, 96-100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi (US Patent 6,286,128) in view of Hossain et al. (US Patent 5,953,236).

Pileggi discloses method for design optimization using logical and physical information including:

(1), (13), (25), (95), (96d) A method, a computer readable medium, a computer system, a semiconductor device, a computer readable medium including code for performing a design of an integrated circuit comprising:

defining a physical design of the circuit while tracking an error (slack or timing "hot spot") in prediction of a timing value associated with one or more nets in the circuit (col.2, ll.57-58; col.3, ll.7-10 and col.6, ll.5-14); and

determining a physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold (col.5, ll.19-48);

(2), (14), (26), (96 c) The method of claim 1, the computer code of claim 13, the computer system of claim 25, a computer-readable medium including a logic structuring module, wherein the defining the physical design further comprises performing a soft placement of the design (col.2, ll.67, col.3, ll.1-2 and ll.25-31);

(3), (15), (27), (100) The method of claim 2, the computer code of claim 14, the computer system of claim 26, the computer readable medium of claim 96, wherein the performing the soft placement of the design further comprises performing one or more of the following: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.2, ll.65-67; col.3, ll.1-5 and ll.38-48);

(4), (16), (28), (99) The method of claim 2, wherein the performing the soft placement of the design further comprises simultaneously performing one or more of the following in parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.2, ll.67 and col.3, ll.1-2 and ll.7-10);

(5), (17), (29) The method of claim 1, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

localizing placement of cells and wires in the physical design (col.8, ll.66-67 and col.9, ll.1-30);

creating a profile of the wire lengths from the physical design (col.9, ll.61-67 and col.10, ll.1-7);

calculating an error in a prediction of a timing value from the profile of the wire lengths (col.10, ll.8-18); and

comparing the error in the prediction of the timing value with the predetermined threshold to determine if the error satisfies the predetermined threshold (col.10, ll.8-18);

(6), (18), (30), (96a), b)) The method of claim 1, wherein the determining the physical placement level of the circuit when the error in prediction of the timing value satisfies a predetermined threshold further comprises:

(a) quadrisectioning the physical design into bins (col.9, ll.16-30);

(b) localizing placement of cells and wires of the physical design into the bins (col.8, ll.15-27 and ll.66-67 and col.9, ll.16-30);

(c) creating a profile of the wire lengths in each of the bins (col.9, ll.61-67 and col.10, ll.1-18);

(d) calculating a plurality of errors in a prediction of timing values from the profile of the wire lengths for each bin respectively (col.7, ll.42-47 and col.10, ll.8-18);

(e) comparing each of the plurality of errors in the prediction of the timing values

with the predetermined threshold to determine if the error satisfies the predetermined threshold; and either:

further quadrisectioning the physical design and repeating (b through e) (col.10, ll.8-18);

or

generating an interrupt if all of the plurality of errors in the prediction of the timing values for each of the bins satisfy the predetermined threshold (col.12, ll.62-64);

(7), (19), (31) The method of claim 6, wherein the creating a profile of the wire lengths in each of the bins further comprises plotting wire lengths versus instances of nets in each of the bins (col.3, ll.10-15);

(8), (20), (32), (96 e)-g)) The method of claim 1, further comprising performing interactive optimization of the physical design after the error in prediction of the timing value satisfies the predetermined threshold (col.2, ll.67; col.3, ll.1-15; col.7, ll.61-67 and col.8, ll.1-4);

(9), (21), (33), (94) The method of claim 1, further comprising analyzing one or more of the following characteristics of the physical design after the error in prediction of the timing value satisfies the predetermined threshold: congestion, timing, power, and signal integrity (col.2, ll.67; col.3, ll.1-15; col.7, ll.61-67 and col.8, ll.1-4);

(10), (22), (34), (97) The method of claim 9, further comprising generating a report indicative of the congestion, timing, power, signal integrity of the physical design (col.10, ll.46-58);

(11a)), (23a)), (35a)) The method of claim 1, further comprising:

performing a second physical design of the circuit derived from the physical design of the circuit performed while tracking the error in prediction of the timing value associated with one or more nets in the circuit (col.13, ll.39-45);

(12), (24), (36) The method of claim 11, wherein the performing the second physical design of the circuit further comprises simultaneously performing one or more of the following in to parallel: placement of cells of the design, logic optimization of the design, routing of wires in the design, timing and clock control for the design and extraction of the design (col.2, ll.67 and col.3, ll.1-15);

(98) The computer readable medium of claim 96, wherein the resource and allocation and sharing module; the implementation module; the logic structuring module; the technology mapping module; the global optimization module; and the prototype optimization tool operate sequentially (col.4, ll.57-67 and col.5, ll.1-3).

4. With respect to claims 11b), 23b), 35b) and 70-79 Pileggi teaches the features above but lacks fabricating a mask and a semiconductor device using above design method of the integrated circuit.

Hossain discloses method and apparatus implementing engineering change orders in integrated circuit design including:

(11b), (23b), (35b) The method of claim 1, further comprising:

generating a GDS file from the second physical design of the circuit (col.2, ll.13-21);

(70)-(79) A method for a first party to fabricate a semiconductor device, comprising:

generating a GDS file from the second physical design (col.2, ll.13-21 and col.4, ll.37-55);

having a mask set generated from the GDS file (col.2, ll.13-21 and col.4, ll.37-55); and

having the semiconductor device fabricated using the mask set (col.2, ll.13-21 and col.4, ll.37-55).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Hossain's teaching regarding fabricating the mask and the semiconductor device using above design method of the integrated circuit to improve the integrated circuit design complexity.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone

numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N L
September 9, 2002

VUTHE SIEK
PRIMARY EXAMINER